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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10081491	FILING DATE 02/22/2002	CLASS 438	SUBCLASS 100	GAU 2812	EXAMINER Roman
<p>**APPLICANTS: Pendse Rajendra; Ahmad Nazir; Chen Andrea; Kim Kyung-Moon; Kweon Young-Do; Tam Samuel;</p>					
<p>**CONTINUING DATA VERIFIED: YES AR 10/30/02 THIS APPLN CLAIMS BENEFIT OF 60/272,237 02/27/2001</p>					
<p>BEST AVAILABLE COPY</p>					
<p>** FOREIGN APPLICATIONS VERIFIED: AR 10/30/02</p>					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO	
Verified and Acknowledged Examiners's initials <i>AR 10/30/02</i>				CPAC 1008-2 US	
TITLE : Chip scale package with flip chip interconnect					

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner			
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
			Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner	
		Applicati n Examiner	
PREPARED FOR ISSUE			
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